Raytheon

High Band Technology Program (HiTeP) Final Report

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1. Introduction and Background for AMRFC High Band Technology Program (HiTeP)

Raytheon is supporting several Navy advanced technology programs. One of the largest to date is the Advanced Multifunction RF Concept (AMRFC) contracts sponsored by the Office of Naval Research (ONR). The motivation for AMRFC is to reduce the surface combatant topside crowding and resulting radar cross section (RCS) by minimizing the number of apertures required to support radar, communications, and electronic warfare (EW) mission needs. AMRFC is an ONR Science and Technology (S&T) Program (part of the Platform Protection Future Naval Capabilities) focused on a future system concept for naval warfare. The AMRFC program endeavors to prove the efficacy of an integrated RF system with minimal apertures and associated electronics to demonstrate radar, communication, and EW capabilities. The goal of the AMRFC program was to demonstrate capability of performing multiple, simultaneous RF functions, including radar, communications and electronic warfare, utilizing a common set of apertures and dynamically reconfigurable hardware. This capability will potentially enhance shipboard electronic warfare and communication capabilities while also reducing the electromagnetic signatures compared to existing ships with their large number of topside apertures.

The AMRFC High Band Technology Program (HiTeP) included the High Band Digital Preprocessor (HBDP) and the High Band Transmit Array (HBTX) Tasks.

The High Band Digital Preprocessor (HBDP) Task developed equipment that was delivered in 2003 under ONR contract number N00014-99C-0314/P00017, item number 0003. The 3-rack equipment consists of the following items: Subsystem Controller, Data Collection Unit, Data Recording Redundant Array of Independent Disks (RAIDs), Narrowband and Wideband RF Downconverters, Narrowband Preprocessors (NBP) and Wideband Preprocessors (WBP), and Power Supplies. The equipment has been integrated into the AMRFC version-1 test-bed at the Naval Research Laboratory (NRL) Chesapeake Bay Detachment (CBD) facilities. The HBDP equipment resides in the upper shelter of the High Band Multifunction Receive System (HBMRS) and has been in use during the integration, test, and demonstration activities of the test-bed system.

The HBTX Task is a proof-of-concept technology demonstration for wideband, multi-function transmit array capabilities to perform communication and electronic attack functions. The main HBTX thrust has been the development of a unique wideband element capable of meeting very challenging AMRFC aperture requirements. The designed radiating element supports an array architecture that consists of sub-arrays with independent beam control and polarization control and correction. Raytheon's preliminary AMRFC wideband radiator design meets or exceeds multifunction aperture requirements over a 6-18 GHz band and has achieved significant performance improvements over other wideband radiators. The radiator design consists of two cross-polarized tapered notch antennas with a balanced feed to increase polarization purity. This wideband (notch) radiator exhibits excellent polarization performance versus scan in principal and diagonal planes (better than any current notch capabilities). It also has achieved unprecedented swept gain performance over a 9:1 bandwidth (2-18 GHz). The radiator is designed to operate from 6 to 18 GHz and will provide, without correction, a cross polarization isolation of 12 dB or better over a 60 degree conical scan volume.

2. Format of this Report

This report is prepared for the Office of Naval Research (ONR) under the contract number N00014-99C-0314/P00017, item number 0004. This report is divided into sections that separately discuss the HBDP Task and the HBTX Task. These tasks were very different in their goals and requirements. The HBDP Task had deliverable hardware and support; whereas, the HBTX had no deliverable items and was a Level-of-Effort (LOE) task focused on technology exploration and development. Both were successful in their goals. This report begins by discussing the HBDP with stated requirements and compliance to those requirements. It also includes a list of presentations and publications, including several charts that appeared in various presentations done for the HBDP task. HBDP is a piece of deliverable hardware currently operating at the Navy's Chesapeake Bay Detachment as part of the AMRFC Testbed. Following the HBDP discussion, the HBTX Task is discussed. We discuss the HBTX technology development, current status, and provide a list of publications, presentations, and patents which resulted from this technology exploration. Also included are the presentation charts delivered at the 2004 Raytheon RF Symposium. These presentations clearly discuss the status of this development effort when the task completed.

In both the HBDP and the HBTX sections, references are made to the various Program Reviews and Technical Interchange Meetings held during this contract. Copies of the electronic versions of these presentations can be provided upon request.

3. HBDP Introduction & Background

This section of the report describes requirements, design approaches and performance of the 3-rack equipment also known as the High Band Digital Preprocessor (HBDP) which, as previously discussed, was delivered in 2003 under ONR contract number N00014-99C-0314/P00017, item number 0003. The 3-rack equipment consists of the following items: Subsystem Controller, Data Collection Unit, Data Recording Redundant Array of Independent Disks (RAIDs), Narrowband and Wideband RF Downconverters, Narrowband Preprocessors (NBP) and Wideband Preprocessors (WBP), and Power Supplies. The equipment has been integrated into the AMRFC version-1 test-bed at the NRL Chesapeake Bay Detachment (CBD) facilities. The HBDP equipment resides in the upper shelter of the High Band Multifunction Receive System (HBMRS) and has been in use during the integration, test, and demonstration activities of the test-bed system.

3.1 HBDP Requirements and Goals

The HBDP equipment supports the AMRFC version-1 test-bed system by performing the narrowband and wideband digital receiving functions and wideband digital beamforming function as depicted in the system block diagram in Figure 1. The HBDP subsystem receives input RF signals from receive antenna sub-arrays in the 6 to 18 GHz band and processes to provide digital outputs for narrowband and digital beam outputs for wideband applications having instantaneous bandwidths of 22 MHz and 230 MHz, respectively. The narrowband data outputs are for downstream narrowband beamforming and the wideband digital beam outputs are for wideband applications. The Narrowband (NB) applications include satellite communication (SatCom) links utilizing commercial Ku-band satellite as well as military satellite, multiple line-of-sight Common Data Link (CDL) and Navigation Radar functions, while the Wideband (WB) applications include a High Gain High Sensitivity (HGHS) Electronic Surveillance (ES) application. The main performance goals of the HBDP subsystem are summarized in Table 1.

3.2 HBDP Design

This section discusses the design process followed for the HBDP development. Details of the Design Reviews, Specifications, and Drawings for this effort are provided in references [7-14].

3.2.1 HBDP Block Diagram

Figure 2 shows a simplified functional block diagram of the HBDP subsystem. The major functions of the HBDP include RF downconversion, narrowband preprocessing, wideband processing, reference signal distribution, hardware control, data collection and data storage.

The HBDP receives 6 to 18 GHz RF signals from sub-array outputs of the receive array through 45 low loss coaxial cables.

Each of the 45 "channels" passes through a high dynamic range RF Downconverter (RF DC) module which performs double downconversion from 6 to 18 GHz to an IF signal of 720 MHz, filtered to bandwidths of 400 MHz and 230 MHz.

A total of 27 channels are further filtered and processed in the Narrowband Preprocessor (NBP) modules for narrowband applications, while the other 18 channels are processed in the Wideband Processor (WBP) units for wideband applications.

Each NBP module processes two NB channels. Each NB channel is downconverted, further filtered, digitized, serialized and converted to send the data over an optical fiber using the G-link protocol [5-6] to the downstream NB Digital Beamformer subsystem.

The 18 WB channels are processed in the Wideband Processor (WBP) units, which perform A/D conversion, digital beamforming, Fast Fourier Transforming, data serialization and optical conversion. A set of 9 WB digitized channels is used to form two simultaneous digital beams, each of which can be output in either the time or frequency domain. Thus, the two WBP units can provide a total of four simultaneous digital beams that are sent over optical fibers to be received and processed by the HGHS ES equipment.

The reference signal distribution assembly receives the reference Local Oscillator (LO) signals, calibration tones and clock inputs from the AMRFC test-bed signal generation unit and distributes these signals to various functional units in the HBDP subsystem.

The HBDP Controller receives operational commands from the AMRFC system Resource Allocation Manager (RAM) to configure the HBDP hardware for real and non-real time operations.

The Data Collection Unit (DCU) of the HBDP subsystem contains 32 channels each with 128 MBytes of high speed buffer memory, and allows real time data collection of 120 MB per second of data per channel. The data from the DCU buffer memory may be sent over fiber to a modular removable 320-GB RAID storage system in the HBDP. The RAID can record approximately 80 one-second slices of data per disc (assuming all 32 channels at 100% duty). The DCU and the RAID may be used to collect and record data from the NB or the WB units of the HBDP.

The laptop PC is used to perform diagnostics by accessing the data in the DCU buffer memory and perform some data analysis.

Figure 3 shows a summary of the HBDP interface signals. Figure 4 shows a photograph of the HBDP subsystem, which is packaged in a modified Commercial Off-the-Shelf (COTS) 3-rack rack assembly providing adequate Electromagnetic Interference (EMI) shielding, safety and interconnect features for test-bed operations.

3.2.2 RF Downconverter Module

Figure 5 shows a functional block diagram and photos of the high dynamic range RF Downconverter module. It performs double downconversion from 6 to 18 GHz to an IF signal of 720 MHz, filtered to bandwidths of 400 MHz and 230 MHz. The front end Low Noise Amplifier (LNA) provides typically less than 6.5 dB of overall Noise Figure (NF) over the 6 to 18 GHz band. The integrated limiter protects the LNA with no damage up to +30 dBm of CW RF input power. The input 1-dB compression level of more than 0 dBm allows operation in the presence of high out-of-band interference signals. The reconfigurable 8-Channel pre-selector allows selection of any of the 8 bands over the 6 to 18 GHz for the particular NB and WB applications. Dual LO operation with selectable second LO allows suppression of undesirable mixer spurious

products [2].

A programmable IF attenuator (0 to 20 dB in 1-dB steps) provides the capability to perform system-level channel calibration and equalization. The downconverter module provides an overall gain of about 30 dB for the NB channel and about 40 dB of gain for the WB channels. The module has provision for greater than 400 MHz bandwidth IF output for future growth.

The RF Downconverter module is of a plug-in type of construction with blind-mate RF connectors and digital signal interfaces to the backplane on a Virtual Machine Environment (VME) based chassis. Each RF Downconverter consumes about 17 W of DC power.

Table 2 shows a summary of typical performances of the 45 downconverter modules.

3.2.3 Narrowband Preprocessor Module

Figure 6 shows a functional block diagram and photos of the Narrowband Preprocessor (NBP) module. Each module processes two NB channels. Each NB channel signal is filtered with a 720 MHz (22 MHz BW) cavity filter before being applied to the NBP module. The module performs single downconversion from 720 MHz to an IF of 75 MHz, and is further filtered to a bandwidth of 22 MHz. More than 70 dB of anti-aliasing filtering is realized by the combined effect of the external cavity filter and the surface mount filter inside the module. Each NB channel is then digitized by a 14-bit A/D converter, and IF sampled at 60 MHz clock rate. Over the 22 MHZ instantaneous bandwidth, the module provides typically greater than 70 dB of Signal-to-Noise-Ratio (SNR). A Field Programmable Gate Array (FPGA) based design is used to insert various test pattern data to help during diagnostic and verification tests. Header data may be inserted at the beginning of each data transmission to help in identifying the data. Each channel utilizes a G-link transceiver chipset to serialize the A/D data followed by fiber optic transmitter chips to send the data over optical fiber at a 1.2 Gigabit per second rate. The digital serial interface to the NBP module is controlled by the HBDP Controller Subsystem as described below. The module provides more than 70 dB of spurious suppression, and over 80 dB of channel to channel isolation. The dual channel NBP module consumes less than 14 W of DC power.

The NBP module packaging consists of a multilayer printed circuit board with surface mount components on both sides, enclosed in a metal housing to realize EMI shielding, blind-mate RF connectors and digital signal interfaces to the backplane on a VME based chassis.

Table 3 shows a summary of typical performances of the NBP modules.

3.2.4 Wideband Preprocessor Subsystem

Figure 7 shows a functional block diagram of the Wideband Preprocessor (WBP) unit that receives 9 wideband channels at 720 MHz, band-limited to 230 MHz, from the output of the RF Downconverters described above. There are two WBP units in the HBDP to process the 18 WB channels. Each WBP unit performs four basic functions: (a) IF to digital conversion, (b) digital beamforming, (c) Fast Fourier Transformation (FFT) and (d) formatting data for transmission over optical fiber. These functions were realized using Raytheon designed ASIC chipsets [3] and unique board designs.

Each of the 230-MHz bandwidth WB channels is digitized by an 8-bit A/D converter operating at 960 MHz sampling rate followed by further digital down conversion. Harmonic suppression of more than 60 dB and an Effective Number of Bits (ENOB) of 7.3 bits were measured. The custom ASIC chipsets allow digital phase, gain and delay adjustments for each of the 9 channels [3]. The amplitude and phase balance among the 9 channels may be adjusted digitally to within less than 0.18 dB and 1 degree, respectively.

Each WBP unit forms two digital beams in the time domain from any or all of the 9 WB channels using programmable weights. The WBP unit also performs time domain to frequency domain processing on each of the two beams using programmable weights and twiddles to produce real-time 512-point FFTs. Either or both of the digital output beams can be selected to be either time or frequency domain data. The WBP provides test pattern insertion at multiple points in the data path to assist in diagnostic and verification tests. Headers are inserted at the beginning of each data transmission to assist in identifying the data. Data is serialized using the G-link serial protocol followed by optical transmitters to send the data over optical fiber. Each digital output beam data is sequentially distributed over a total of 8 fibers each at a serial data rate of about 1.2 Gigabits per second.

3.2.5 Data Collection Unit (DCU)

Figure 8 shows a functional block diagram of the HBDP Data Collection Unit (DCU). Figure 9 shows photos of the various elements of the DCU. It receives 32 channels of fiber optic serial data, selectively stores this data in channel memory, and transfers the channel memory content to a mass storage device such as a RAID. It also provides external command and status interface.

The source of the 32 serial channels is a fiber optic switch external to the HBDP. The NRL fiber optic switch sends either 32 WBP channels or 27 NBP channels as inputs to the DCU. A Fiber Channel connection provides a data path to and from the RAID mass storage device. A Systran FibreXpress Peripheral Component Interconnect (PCI) Mezzanine Card (PMC) module on the Single Board computer (SBC) provides the Fiber Channel connection. FibreXpress is a trademark of Systran Corp. and is an ANSI standard Fiber Channel network implemented over a 1.0625 Gbit/sec Fiber Channel.

The DCU consists of a VME64x chassis containing 16 Receiver Memory CCA's and an SBC. The DCU receives 32 channels of serial data and captures this data in channel memory. The SBC controls transfer of captured channel memory data to mass storage via FibreXpress. The Ethernet connection to the SBC provides a data path for control messages to and status messages from the DCU.

Each Receiver Memory module contains two fiber G-link receive channels, two channel memories, a VME64x interface and a 60MHz clock distribution circuit. One Receiver Memory module receives 60MHz reference sine wave and distributes 60MHz clock signals to all Receiver Memory modules. Internal timing signals are derived from this 60MHz clock. The Receiver Memory receives two G-link fiber channels and is capable of capturing into the channel memory 128M bytes of real time receive data. VME interface has read/write access to channel memory. Channel memory tracks the amount of captured data. The Receiver Memory acts as a VME64x slave and recognizes its address space by geographic and broadcast addressing.

The SBC is a COTS 366MHz Power PC based with 256M byte RAM and 8M byte flash memory. The Motorola MVME2700 series was chosen as the standard SBC for AMRFC. The SBC contains a 10/100 Base –T Ethernet port and PMC site. The PMC site contains the Systran FibreXpress interface module. The FibreXpress interface is capable of 100M Byte per second data transfer rate. The Ethernet port requires a P2 Adaptor and cable mounted on the rear of the backplane and a Transition Module in slot 2. The SBC is the VME64x bus master and resides in slot 1.

The modules within the DCU communicate over a VME64x bus. Geographic addressing allows each Receiver Memory to determine its card slot position in the backplane and defines the address space for each Receiver Memory.

The DCU provides a Fiber Channel interface to the mass storage device. The DCU outputs data in a standard file format compatible with the software operating system. Each output file is identified with DCU channel number and dwell number. The size of each file is determined by the number of message bytes (header plus data) captured in channel memory since the last arm/disarm sequence.

The DCU is contained in a 21-slot VME64 chassis that is 14 inch high and a 19 inch rack mount unit. The chassis provides DC power and forced air cooling to the modules. External connections to the DCU are on the module front panels with the exception that AC Power and 60 MHz Reference are rear panel connections.

3.2.6 Local Oscillator (LO) and Reference Signal Distribution

The following Local Oscillator (LO) and Reference signals are distributed inside the HBDP:

(a) First and Second downconversion LOs to the RF Downconverters
(b) Third downconversion LO to the Narrowband Preprocessor
(c) RF calibration signals to the RF Downconverters
(d) IF calibration signals to the NB preprocessors and WBPs
(e) A/D reference clocks of 60 MHz to the NBP and 960 MHz to the WBPs

Distribution of the nine (9) Narrowband LO1 signals (11-23 GHz) from the cabinet input interfaces to the 27 downconverters includes amplification, power level detection and fault reporting for each amplifier path and use of low loss RF cables.

Distribution of the two (2) wideband LO1 signals (11-23 GHz) from the cabinet input interfaces to the 18 downconverters includes amplification, power level detection and fault reporting for each amplifier path and use of low loss RF cables.

Distribution of the Downconverter LO2A/B second LO signals (5.22/5.72 GHz) from the cabinet input interfaces to the 45 downconverters includes amplification, power level detection and fault reporting for each amplifier path and use of low loss RF cables.

Distribution of the Narrowband LO3 signals (795 MHz) for third LOs from the cabinet input interfaces to the 27 Narrowband Preprocessors channels includes amplification, power level detection and fault reporting for each amplifier path and use of low loss RF cables.

Distribution of the RF Calibration signals (6-18 GHz) from the cabinet input interfaces to the 45 downconverters includes use of low loss RF cables, RF connectors, power dividers etc... One-time amplitude/phase calibration of the entire distribution network including all cables was performed to create correction tables for use during system calibration.

Distribution of the IF Calibration signals (720 MHz) from the cabinet input interfaces to the 27 narrowband channels and 18 wideband downconverters uses passive components only. The IF calibration signal provides intermediate test tone injection points to help troubleshoot and isolate any channel failures up to the least replaceable units. This was also used during integration and test phase for preliminary checkout and to verify channel tracking and beamforming capabilities at the IF level.

Distribution of the Reference signals (60 MHZ) from the cabinet input interfaces to the 27 Narrowband Preprocessor channels, Controller and the DCU includes amplification, power level detection and fault reporting for each amplifier path and use of low loss RF cables.

3.2.7 Subsystem Controller

The Subsystem Controller consists of a VME enclosure and backplane populated with a SBC, Hardware Controller (HC) modules, VME Repeater modules, and power supplies. Software resident on the SBC initializes controls and provides status of the HBDP hardware which consists of RF Downconverter (RF DC) modules, Narrowband Preprocessor (NBP) modules, Wideband Preprocessor (WBP) assemblies and the Data Collection Unit (DCU). The SBC receives real time commands over a serial fiber data link and non-real time commands over an Ethernet link from the AMRFC system RAM. A custom VME backplane provides the interface between the SBC, HCs and VME Repeaters. The HCs are FPGA based designs and control the RF DC and NBP modules using Low Voltage Differential Signaling (LVDS) serial interfaces. Each serial interface controls multiple modules using a party line (multi-drop) bus arrangement. A master HC generates a synchronous one millisecond (programmable for multiple of 1 millisecond) period internal timing signal based on the system timing strobe and uses this internal signal to initiate SBC software activity, output party line commands and control application of these commands to the HBDP hardware. The WBP assemblies receive initialization and control data from the SBC through the VME Repeater interface.

The HBDP Controller also performs non-real time calibration and diagnostics as per instructions received from test-bed RAM over the Ethernet. The HBDP Controller reports the calibration data, diagnostics results, and status to the RAM over the Ethernet.

3.2.8 HBDP Mechanical Design

HBDP is packaged in three heavy duty 19 inch equipment racks of 30 inches deep (COTS, with modifications). The cabinets were manufactured by Equipto Electronics Corporation. The three cabinets were attached together to form a 3-rack unit (no interior partition panels). The cabinets were constructed of stainless steel to reduce corrosion and have front doors and rear panels to provide EMI shielding. All electrical connections enter through the top rear of the cabinet.

The electronics in the three racks are cooled by forced air convection. Each cabinet has inlet vents on the front door and exhaust fans on the top surface. Each chassis has fans, properly sized

according to heat loads, to push or pull external air over modules and power supplies, and exhausts to interior of the cabinets.

The following were design goals:

Temperature Non-operating:	14 to 149 degrees F (-10 to +65 degrees C)
Temperature Operating:	OHSA Office Standard (65 to 76 degrees F)
Vibration:	Normal Commercial Transportation Standards
Humidity Non-operating:	10% to 95%, no condensation
Humidity Operating:	10% to 80%, no condensation
Altitude Non-operating:	Sea level to 40,000 feet
Altitude Operating:	Sea level to 3,000 feet
Cooling Conditioning:	For total heat load of 10 kW (Max)

Cabinets were designed to be installed through equipment door and bases allow fork-lift pickup. Cabinet frames are installed and assembled with internal cables. Cabinets are fastened to shelter floor. Suitable locations were available to allow the addition of top sway bracket. Cabinets draw in cooling air from front surface and vent heated air at rear and top surfaces. Overhead wiring raceways were available for all cabling.

Power Distribution Units on each rack contain circuit breakers and power indicators.

The Downconverter Assembly Chassis is based on APW Titan VME64x chassis, modified by increasing depth of sidewalls 120 mm to use 6U x 280 module form factor. Other modification was made to increase number of fans from 2 above to 3 below. Motherboard consists of RF interconnect plate combined with Printed Wiring Board (PWB) motherboard and supports 15 modules, 6U x 280, on 1 inch pitch.

Narrowband Preprocessor Assembly is based on APW Titan VME64x chassis, modified by changing mounting brackets to set front panel back 2 inches into cabinet to provide clearance for front mounted fiber-optic cables. Modification was made to increase fans from 2 above to 3 below. Motherboard is similar in design and construction to the one in the downconverter assembly and supports 15 modules, 6U x 160, on 1 inch pitch.

Subsystem Controller is based on APW Titan chassis modified to use the set-back mounting brackets but with standard fan arrangement. The Motherboard is a custom VME64x backplane.

Data Collection Unit is based on APW Titan chassis modified to use the set-back mounting brackets but with standard fan arrangement. Motherboard is a COTS VME64x backplane.

Wideband Preprocessor assembly is based on custom Mupac chassis, custom backplane, mounts on slides, and uses 7 fans. Module access is from top of the unit. Filter assembly is a shielded purchased assembly.

LO Distribution modules are open bay type.

RF Downconverter Module is based on 6U x 280 module form-factor, but uses 1 inch pitch. Blind mate OSP and OSSP type RF connectors mounted in backplane provide radial float feature. Power/signal connector is a 50 pin D style (metal body Mil-C-24308 type). The module is a shielded EMI enclosed module, contains 0.15 inch cooling fins on one side of module, 25 watts max dissipation, IEEE 1101.10 extractors on panel to aid removal.

NB Preprocessor Module is based on VME64x 6U x 160 module form factor on 1 inch pitch. Each NBP module is a two-sided surface mount construction, contains two RF channels per module, uses EMI shielded covers, and designed for 16 watts of power dissipation. Blind mate OSP coax connectors and 50 pin D connector mate with backplane. SC style fiber optic (FO) connectors are thru the front panel. Extractors are on the front panel to aid module removal.

3.2.9 HBDP Software Control (HSC)

The interface to the HSC software is described in Figure 10 and its major capabilities are described in the following:

All system tasks are spawned by a UNIX startup script initiated by the AMRFC Test-bed operator through a VxWorks Windshell. The HBDP Embedded Controller Software (ECS) is made up of the following:

a. NRL's Real Time Network Control (RTNC) Application Program Interface (API) Software
b. General Dynamic's Digital System Resources (DSR) Middleware Software
c. Raytheon's HBDP Software Controller (HSC) Software

Additionally, Raytheon has provided two other operational software programs in support of the HBDP Data Collection Unit (DCU):

a. Data Collection Unit Software Program (DCU)
b. Laptop Diagnostics Program (LTOP)

Like the HBDP Embedded Controller Software, the DCU tasks are spawned through a VxWorks Windshell, however the LTOP is initiated through a UNIX program startup command and its primary function is to provide non-real time diagnostics for the DCU.

HSC functions are called from the HSC main to initialize the HBDP and enable it to respond to Resource Allocation Manager (RAM) requests. This software supports both real time and non-real time processing.

When the software is operating in real time, it filters and tests real time commands from the AMRFC Test-bed RAM and uses data from these commands to provide inputs to the HBDP hardware. These inputs will enable the hardware to digitize the incoming waveforms and provide these as outputs to the AMRFC system. The digitized output data of each of the Narrowband and Wideband Preprocessors is passed to the G-link Fiber Optic Distribution Unit (GFOD). Subsets of the data can also be stored on the system hard disk through the DCU upon request from the AMRFC Test-bed RAM. HSC status is returned to the AMRFC Test-bed RAM when a change in status is detected or when specifically requested by the AMRFC Test-bed RAM.

As part of the AMRFC system calibration, the Test-bed RAM may request for WBP calibration data stored in the DCU to be transferred to the Test-bed Signal and Data Processor (SDP).

When the software is operating in non-real time, the HSC software can update HBDP configuration software tables, perform diagnostic testing of the HBDP, process commands for the DCU, and provide for status to be sent to the AMRFC Test-bed RAM upon request.

As part of the HBDP Sell-Off Acceptance Test the HSC, DCU, and LTOP software programs successfully met all current software requirements.

To support AMRFC system calibration modes 4, 10, and 19, the HSC software originally provided the processing required for obtaining, re-formatting and transferring the WBP calibration data from the DCU to the SDP. During the integration support effort at CBD, per NRL request and guidance, the HSC program and the DCU program were updated to initiate this functionality from HSC and utilize the DCU to perform all processing involved in reformatting and transferring the WBP calibration data to the SDP. This enabled the calibration effort to be much more efficient, off-loading time-consuming processing efforts from the HSC to the DCU. Several other software modifications were made as part of the system integration support effort at CBD.

3.3 HBDP Integration and Test

3.3.1 Integration and Test

The HBDP integration flow consisted of many sequential and parallel tasks. After the cabinet modifications, AC wirings were installed followed by installation of the power supplies, distribution assemblies, the Subsystem Controller Unit and the Data Collection Unit. Safety inspections were performed at various steps as required by Raytheon Safety Engineering standards. The Government Furnished Equipment (GFE) software development station was utilized to test and integrate various software functions in the HBDP. Once the Subsystem Controller functionality was verified, the remaining assemblies were integrated into the cabinets in parallel after these were separately tested out on the bench. The NBP assembly, RF Downconverter assemblies, and the WBP assemblies were integrated and incrementally tested to verify critical performances. The narrowband channels interface tests with the NRL narrowband beamformer were verified in a joint performance demo with NRL personnel.

3.3.2 Calibration

The HBDP contains built-in passive RF distribution hardware for calibration purposes. This distribution assembly can accept an external calibration signal and couple it into the inputs of all of the 45 downconverters. An external passive distribution assembly, which is independently calibrated, is then used to inject the same signals into the HBDP channel inputs. The data from both sets of measurements are then used to calculate the complex coupling coefficients of the internal RF distribution hardware. These correction factors are stored in the HBDP's calibration files and used (under software control) during subsequent system calibration measurements [4].

3.3.3 HBDP Performance

The performances of the HBDP were measured to meet the key system requirements [2] shown in Table 1. The functions of HBDP subsystem are controlled by software. Upon command, as

specified by the resource allocation message, the hardware in each "channel" is configured to (a) receive the RF signal from a specified sub-array of the receive arrays, (b) pre-select the specified band for NB or WB application, (c) apply specified attenuator settings and (d) send either test pattern, digitized NB digital data, or WB digital beam data to the specified destination.

Figure 11 shows typical performance of a NB channel when a single frequency RF signal is applied at the input of the HBDP. The digital output is collected by the DCU and the data is analyzed using the laptop. The NB channels provide greater than 60 dB of dynamic range over the processing bandwidth of 22 MHz. Adjacent NB channel isolation is better than 80 dB.

Figure 12 shows typical performance of the WB channels. As, mentioned earlier, a set of 9 WB channels are processed by each WBP unit, to form two digital beams. The Spurious Free Dynamic Range (SFDR) of the WB channels (after beamforming) is better than 45 dB over the processing bandwidth of 230 MHz. Adjacent WB channel isolation is better than 40 dB.

The overall Noise Figure (NF) of all the channels is typically 4.5 dB at 6 GHZ to 6.5 dB at 18 GHz. The HBDP can handle a maximum of +30 dBm of CW RF power input without damage.

The overall AC power consumption by the 3-rack cabinet equipment was measured to be less than 6000 Watts compared to a specified maximum of 8000 Watts. The worst case temperature rise from the inlet to the exhaust air flow was measured to be less than 10 degrees F.

3.3.4 HBDP Integration into the AMRFC Test-Bed System

Raytheon worked very closely with the NRL personnel during shipping and installation of the HBDP equipment, first at the NRL facilities in Washington during June to Sept 2003 and subsequently at the CBD test-bed facilities. Raytheon team members traveled to the site as frequently as required. The detailed hardware check-out was performed jointly with NRL personnel.

During the period of AMRFC test-bed integration, test and demonstration activities at CBD, Raytheon software engineers worked very closely with the NRL personnel and responded promptly in making changes in software to adapt to the system software build upgrades.

3.4 HBDP Conclusions

Raytheon designed, developed and delivered a fully integrated very wide band digital receiver subsystem, known as HBDP, to support the ONR/NRL AMRFC test-bed program. The equipment was completed and delivered on schedule and within budget. Raytheon also supported during hardware and software integration, test, and validation of the HBDP in the test-bed system which successfully completed its demonstration phase in November 2004.

3.5 HBDP Publications and References

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[3] William D. Weaver, "Raytheon General-Purpose Wideband Digital Receiver," GOMAC Conference, March 2001, San Antonio, TX.

[4] de Graaf, J., Tavik, G., Bottoms, M., Tatum, C., "Calibration overview of the AMRFC test bed," IEEE International Symposium on Phased Array Systems and Technology, 2003, 14-17 Oct. 2003. pp. 535-540.

[5] Data sheet and application note, 2000, Agilent HDMP-1032/1034 Transmitter/Receiver chipset.

[6] Data sheet and application note, Fiber Optic Transceiver for Gigabit Ethernet, Agilent HFCT-5912E and HFCT-53D5 family.

[7] AMRFC HBDP Final Hardware Design Review (FHDR) handout package, 24-25 October 2001.

[8] AMRFC HBDP Test Requirement Review (TRR) handout package, 16 July 2002.

[9] AMRFC HBDP Acceptance Test Plan (TPH291092)

[10] AMRFC HBDP Acceptance Test Data Package

[11] HBDP Top Assembly Drawing (H291092)

[12] HBDP Prime Item Development Specification (B1) H292299

[13] Software Requirements Specification for AMRFC HBDP Subsystem Controller (H291087)

[14] Interface design Description for AMRFC HBDP Subsystem Controller (HSC), H292300

3.6 HBDP Performance Tables

The tables contained in this section outline the basic performance goals for the HBDP system (Table 1) as well as the individual performance of the HBDP Down-converter module (Table 2) and the HBDP narrowband preprocessor module (Table 3).

Table 1: HBDP Performance goals

Performance Parameters	Requirement and Goals	Comments
Operating Input Frequency range	6.0 to 18.0 GHz	Compliant
Number of channels	45 (Narrowband=27, Wideband=18)	Compliant
Maximum Protection level	+30 dBm CW	Compliant
Recovery Time from Saturation	10 usec max for +30 dBm input power	Compliant
Reconfiguration time	1 usec max	Compliant
Channel Isolation	> 60 dB (NB), > 40 dB (WB)	Compliant
Third-order Intercept (Input)	0 dBm (Narrowband), -10 dBm (Wideband), min	Compliant
Noise Figure	6.5 dB (w/o the array cables)	Compliant
Noise Floor Input	-97.5 dBm to -105.3 dBm	Compliant
Gain Adjustment	20 dB in 1 dB steps	Compliant
RF Front-end compression	0 dBm min	Compliant
Narrowband Processing bandwidth	22 MHz (-3-dB), 38 MHz (-70-dBmin)	Compliant
Narrowband Channel Tracking	+/- 1 dB, +/- 10 degree Peak-Peak	Compliant
Narrowband Dynamic Range	60 dB min (A/D FS to 22 MHz RMS Noise)	Compliant
Narrowband Intermodulation Spurious	Mixer products <-50 dBc, <-30 dBc (2-tone @ -6 dBFS	Compliant Compliant Compliant
Wideband Processing Bandwidth	230 MHz (-0.5-dB), 480 MHz (-50-dB)	Compliant
Wideband Channel Tracking	+/- 1 dB, +/- 5 nS	Compliant
Wideband Dynamic Range	45 dB min after beamforming (A/D FS to 250 MHz RMS Noise)	Compliant
Wideband Intermodulation Spurious	Mixer products <-50 dBc, <-40 dBc (2-tone @ -6 dBFS	Compliant Compliant

Table 2: HBDP Downconverter Module Performance						
S/N	NF (dB)	NF (dB)	IM3 (-6dbm ea)	Ret Loss (RFin)	Group Delay (ns) at	
CS-xxxx	(<14 GHz)	18 GHz	dBc (8db Att)	(> dB)	IF1	IF2
1887	5.5	6.8	53.0	12.0	27.0	19.4
1888	5.5	7.0	50.8	8.7	26.9	19.4
1889	6.0	7.5	48.0	8.4	27.3	19.4
1990	5.6	7.5	49.0	8.2	26.7	19.7
1991	5.7	7.7	51.8	7.3	26.0	19.1
1992	6.0	7.7	53.3	8.3	26.0	19.3
1993	6.0	7.5	51.6	8.1	26.8	19.6
1994	5.7	6.8	50.3	8.7	26.9	19.6
1995	5.6	6.8	49.5	7.4	27.2	19.5
2200	5.3	6.8	46.5	8.2	28.6	24.0
2201	5.5	7.5	43.0	8.2	24.9	17.3
2202	5.2	7.0	46.4	8.7	24.9	17.3
2203	5.0	6.7	47.4	8.8	28.4	19.2
2204	5.5	6.7	47.9	8.8	23.4	15.6
2205	5.5	6.5	46.0	7.0	24.0	16.0
2206	5.2	7.0	45.9	7.1	24.4	15.7
2207	5.5	7.0	46.7	7.8	24.9	17.4
2208	5.0	6.0	45.6	10.7	25.5	16.6
2209	5.4	6.6	47.6	8.6	28.6	19.5
2210	5.6	7.0	47.7	9.7	25.0	17.2
2211	5.5	7.0	50.3	8.5	25.8	17.8
2212	5.8	6.8	50.7	8.2	29.7	25.5
2213	5.5	6.5	46.9	8.6	24.9	17.1
2214	5.5	6.5	47.6	7.5	24.9	17.2
2215	5.7	6.8	47.7	8.2	24.9	17.6
2216	6.0	7.5	50.8	6.5	24.8	17.9
2217	5.5	7.0	50.2	8.3	24.9	17.6
2218	5.5	6.8	47.7	8.2	24.6	17.6
2219	5.7	7.5	45.7	6.7	25.0	17.6
2220	5.8	7.0	49.0	7.3	24.4	17.4
2221	5.5	7.3	46.2	8.4	24.9	17.8
2222	5.5	7.3	48.3	8.2	24.6	17.4
2223	5.5	7.3	48.8	7.6	24.8	17.7
2224	5.5	6.8	47.0	8.4	24.9	17.8
2225	5.0	6.5	48.7	8.4	24.7	17.5
2226	5.3	6.4	52.3	7.6	24.4	17.3
2227	5.5	6.8	49.3	8.5	24.6	17.6
2228	6.0	8.0	47.2	8.3	24.6	17.7
2229	6.0	7.5	51.8	7.8	24.5	17.1
2230	6.0	7.5	51.3	7.3	25.0	17.8
2231	6.0	6.5	57.8	7.9	24.9	17.6
2232	5.3	6.8	47.7	8.1	24.5	17.4
2233	5.6	6.8	47.7	7.2	24.7	17.9
2234	5.5	6.7	50.5	7.0	24.5	17.5
2235	5.5	7.0	45.7	9.0	24.5	17.5
Mean	**5.6**	**7.0**	**48.8**	**8.2**	**25.5**	**18.2**
Std Dev	**0.27**	**0.42**	**2.62**	**0.95**	**1.38**	**1.76**

Table 3: HBDP, Narrowband Preprocessor (NBP) Module							
Signal to Noise Ratio (SNR) performance summary							
Module	**SNR (dB)**	**SNR (dB)**	**mA @**	**mA @**	**mA @**	**mA @**	**mA @**
Serial No.	**Ch. A**	**Ch. B**	**+ 15V**	**+ 8V**	**- 8V**	**+ 5V**	**+ 3.3V**
S/N 0001	71.4	71.2	310	720	50	40	660
S/N 0002	71.0	71.5	310	700	50	40	700
S/N 0003	71.6	71.6	330	700	50	40	700
S/N 0004	71.7	71.4	333	710	60	40	680
S/N 0005	71.5	71.4	330	730	60	40	690
S/N 0006	71.2	71.4	360	710	50	40	690
S/N 0007	71.4	71.6	330	770	50	40	710
S/N 0008	71.6	72.2	333	740	50	40	700
S/N 0009	71.4	71.9	320	740	60	40	720
S/N 0010	71.2	71.2	320	730	60	40	720
S/N 0011	71.2	71.5	320	750	50	40	700
S/N 0012	70.5	71.5	330	765	60	40	720
S/N 0013	71.6	71.6	390	690	50	40	590
S/N 0014	71.2	71.7	330	740	50	40	710
S/N 0015	71.3	71.5	320	695	46	41	665
S/N 0016	71.6	71.5	320	710	50	42	650
S/N 0017	71.7	71.6	320	710	50	42	650
Min.	**70.5**	**71.2**	**310**	**690**	**46**	**40**	**590**
Max	**71.7**	**72.2**	**390**	**770**	**60**	**42**	**720**
Std Deviation	**0.30**	**0.22**	**18.7**	**23.3**	**4.8**	**0.7**	**32.9**

3.7 HBDP Figures and Presentation Charts

The Figures in this section are referred to in the main body of the text discussing the HBDP system and are vu-graphs from some of the various HBDP presentations.

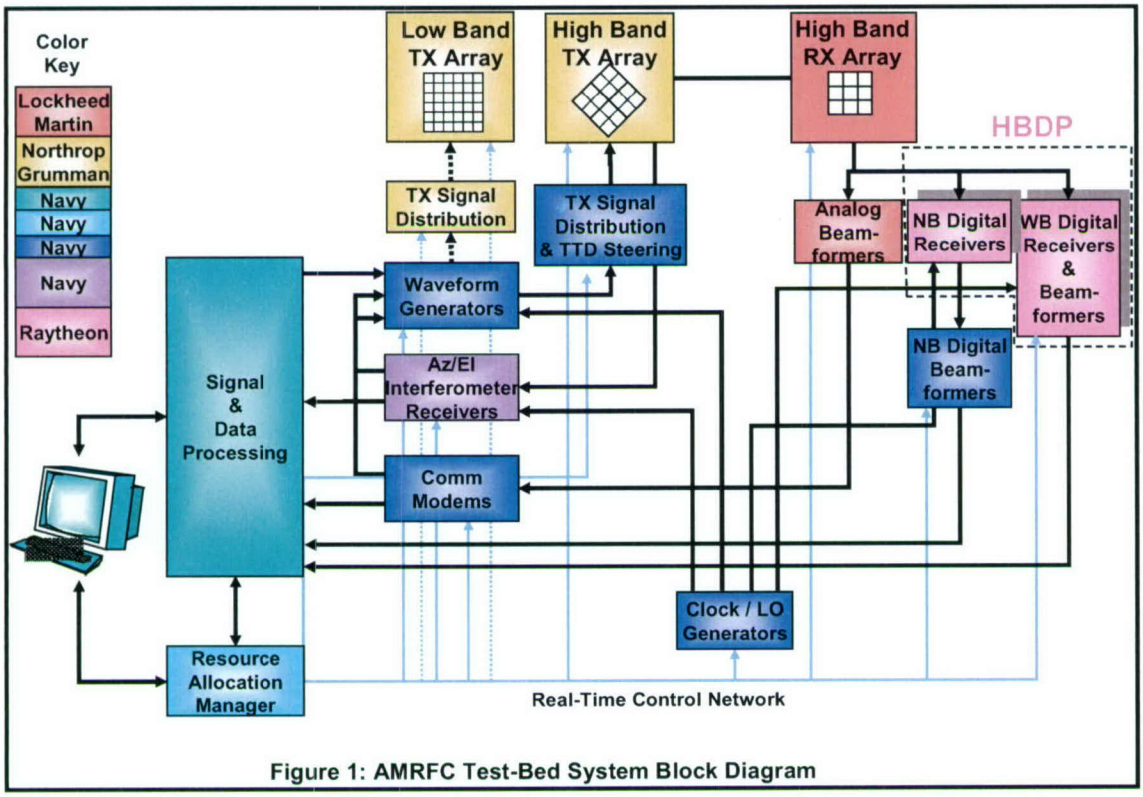

Figure 1: AMRFC Test-Bed System Block Diagram

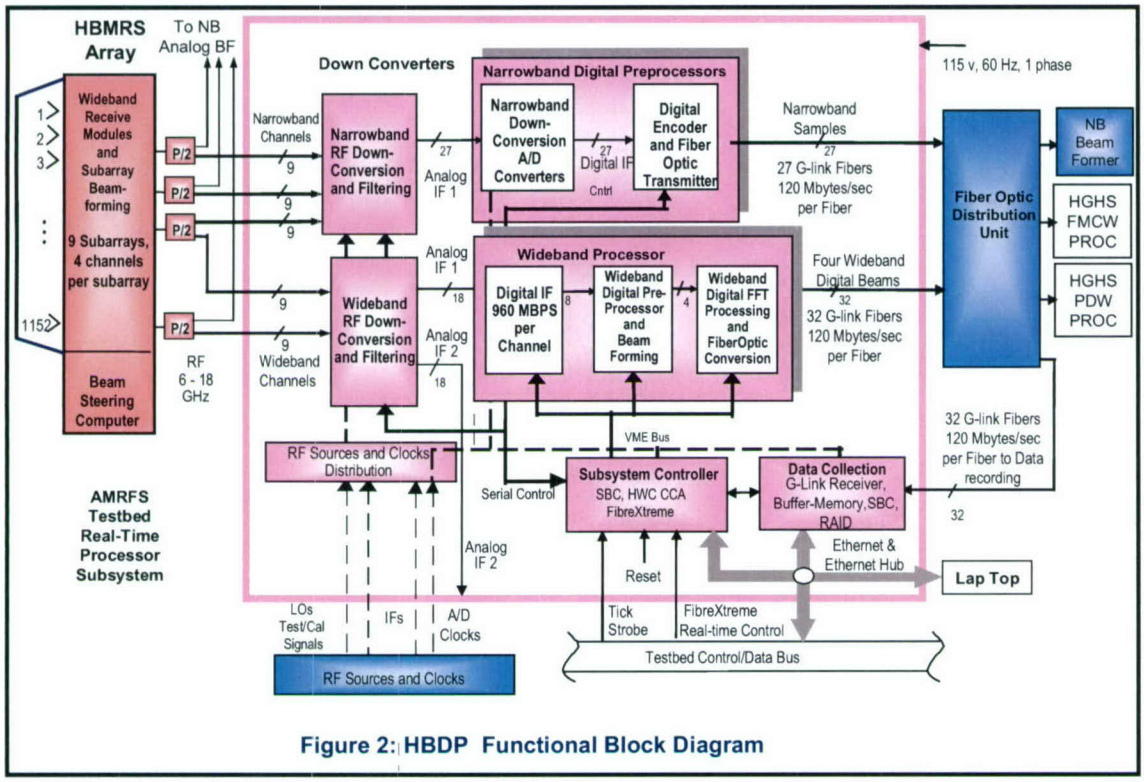

Figure 2: HBDP Functional Block Diagram

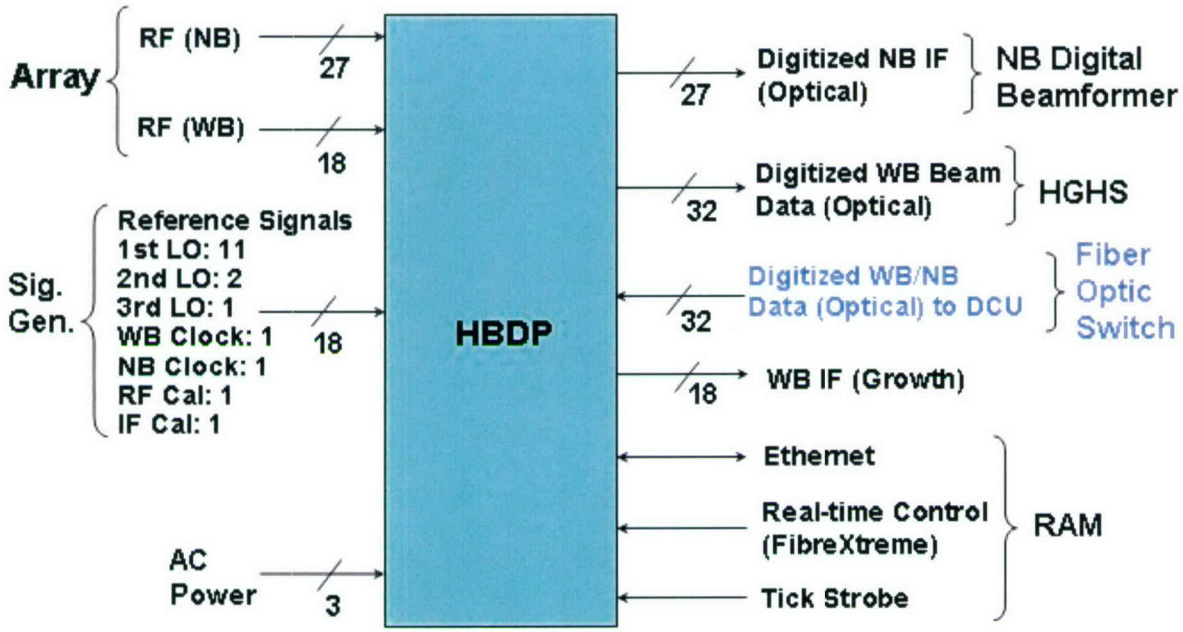

Figure 3: HBDP Interface Summary

- HBDP subsystem equipment installation in the upper HBMRS Trailer
  - 3 Bay COTS EMI Cabinet, VME Chassis and Custom Backplanes
  - 500 RF Cables and 100 Optical Fiber Cables

Figure 4: HBDP Hardware Packaging and Configuration

- Downconversion from 6-18 GHz to 720 MHz (BW of 400 MHz and 230 MHz)
- Reconfigurable 8 pre-select bands, selectable LO, IF Attenuator
- Typical noise figure less than 6.5 dB over 6 to 18 GHz, Gains 30 dB (NB) and 40 dB (WB)
- 1" pitch plug-in module in VME based chassis, OSP RF Connectors Blind-mate to Backplane,

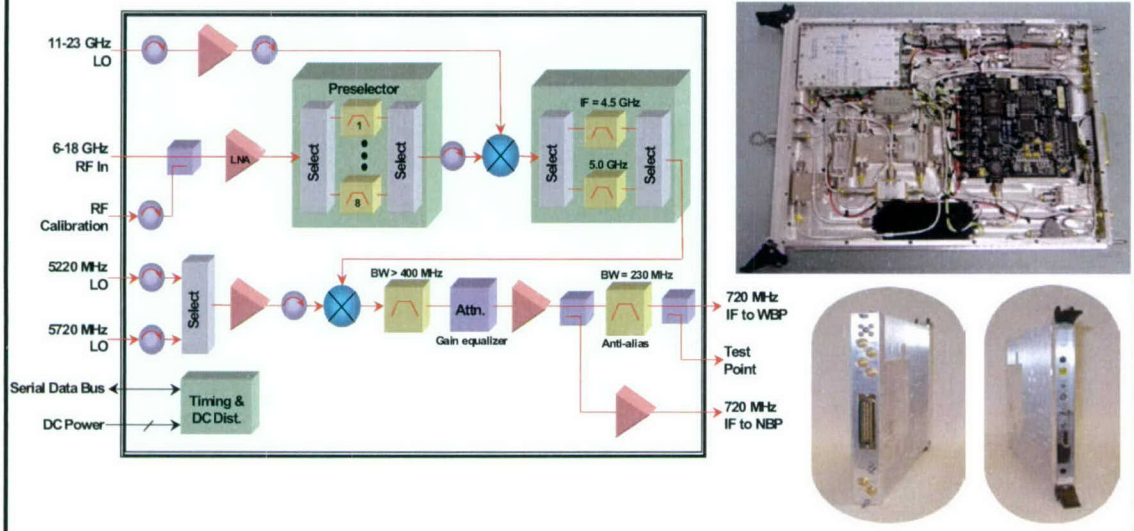

Figure 5: RF Downconverter Functional Block Diagram and Photos

- Downconversion from 720 MHz to 75 MHz (BW of 22 MHz)
- OSP RF Connectors Blind-mate to Backplane
- 1" pitch plug-in module in VME based chassis
- 14-Bit A/D, 60 MHz sampling, > 71 dB SNR over 22 MHz
- Spurious suppression > 70 dB, Channel-Channel Isolation >80 dB

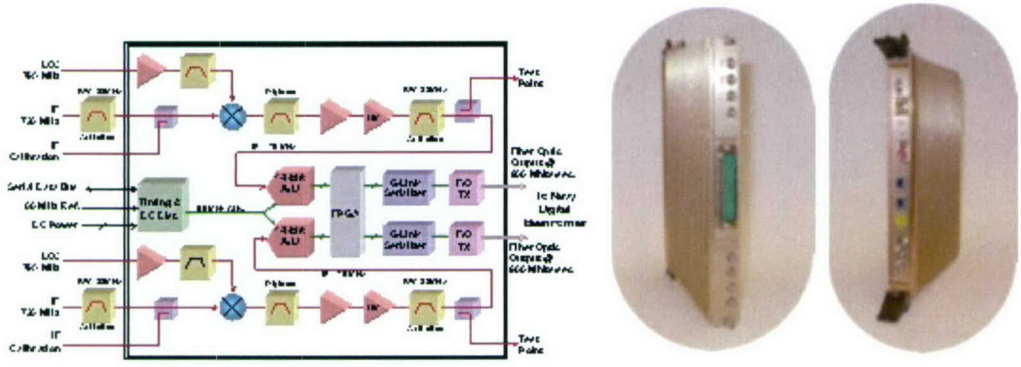

Figure 6: Narrow Band Preprocessor (NBP) Functional Block Diagram and Photos

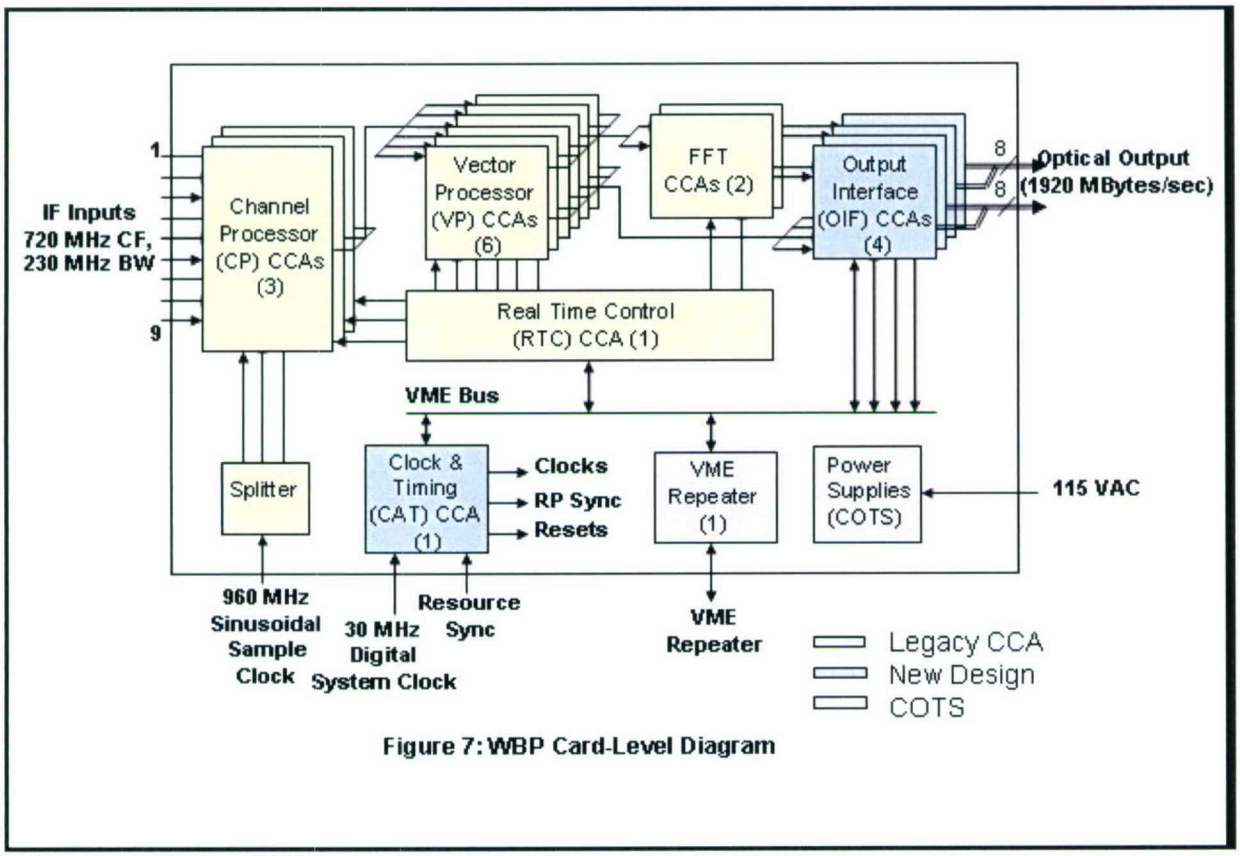

Figure 7: WBP Card-Level Diagram

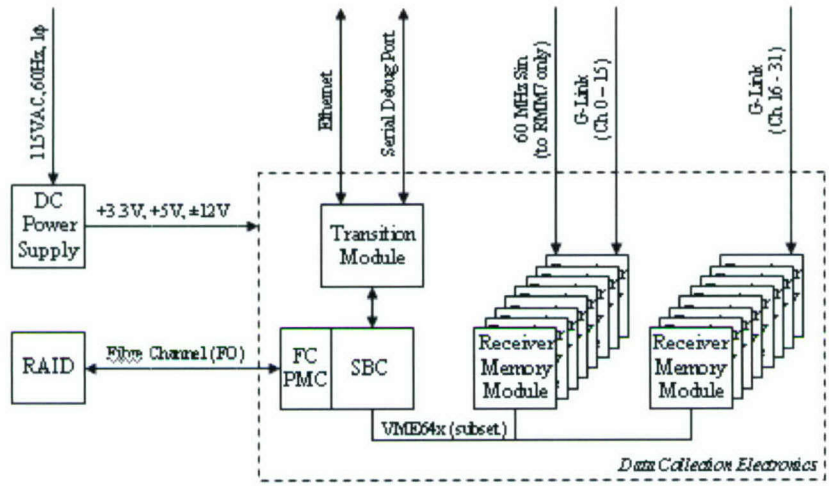

Figure 8: Data Collection Subsystem Functional Block Diagram

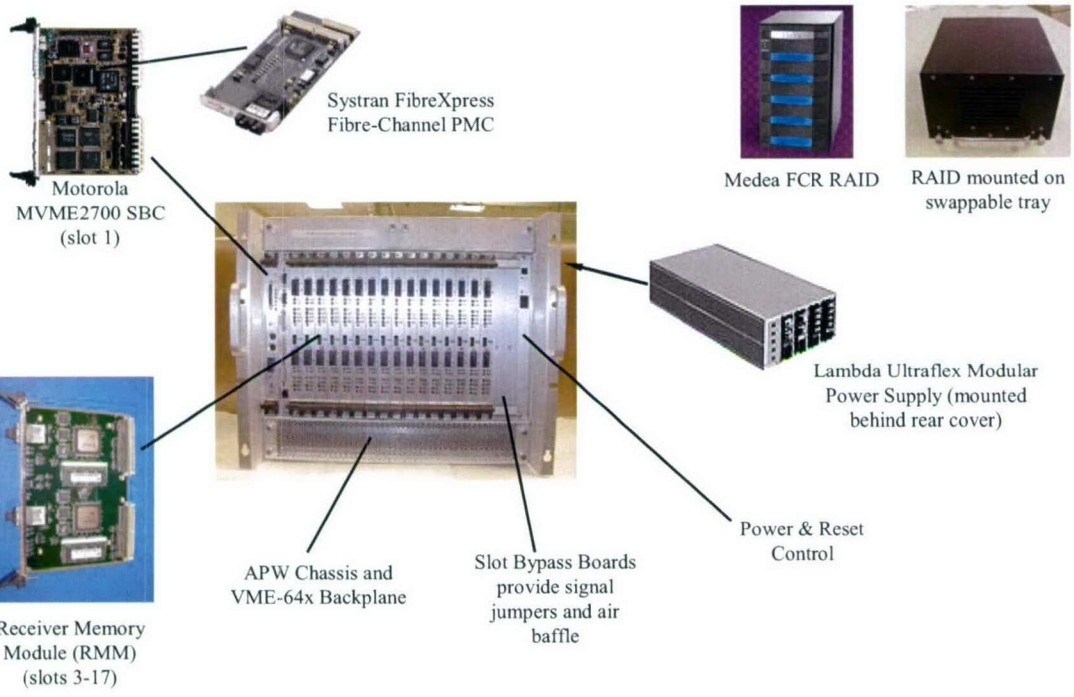

Figure 9: Data Collection Subsystem Elements

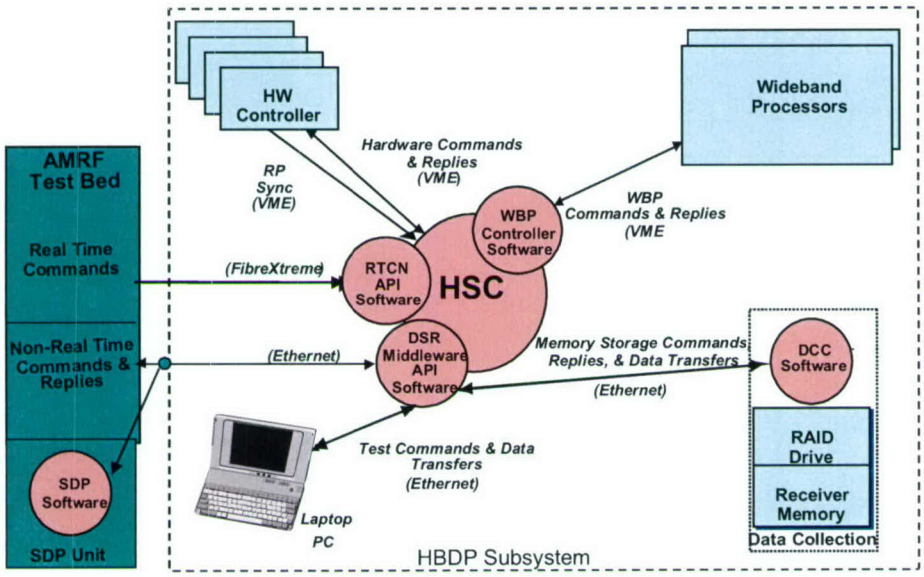

Figure 10: AMRFC HBDP SW Interface Diagram

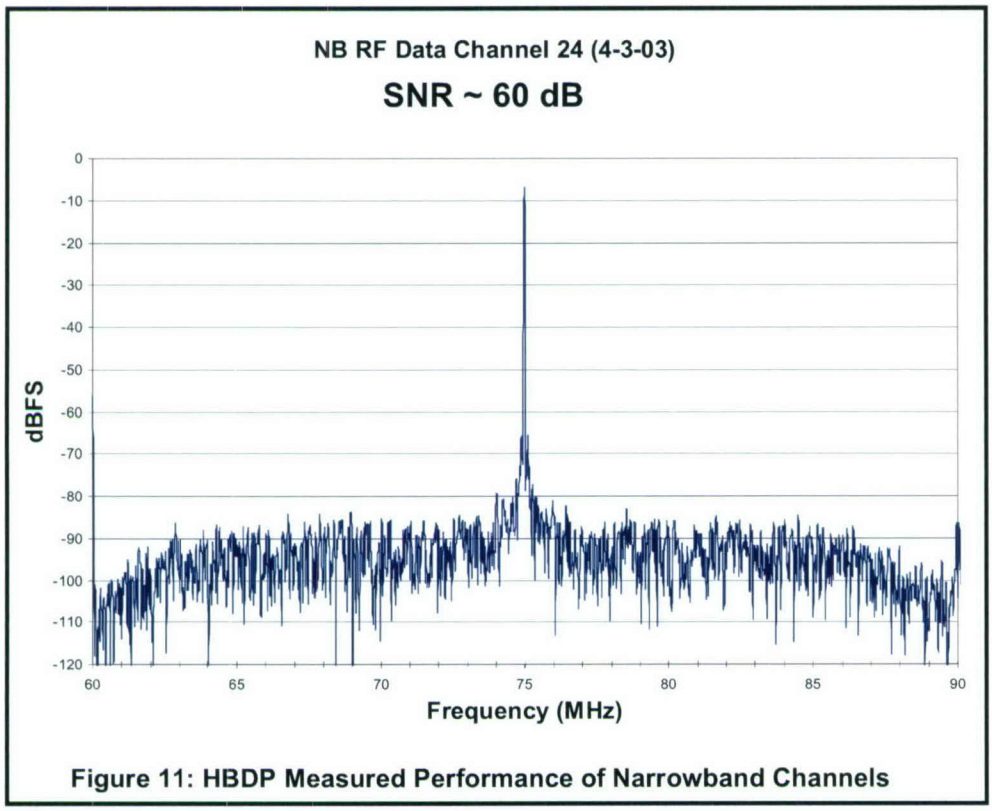

Figure 11: HBDP Measured Performance of Narrowband Channels

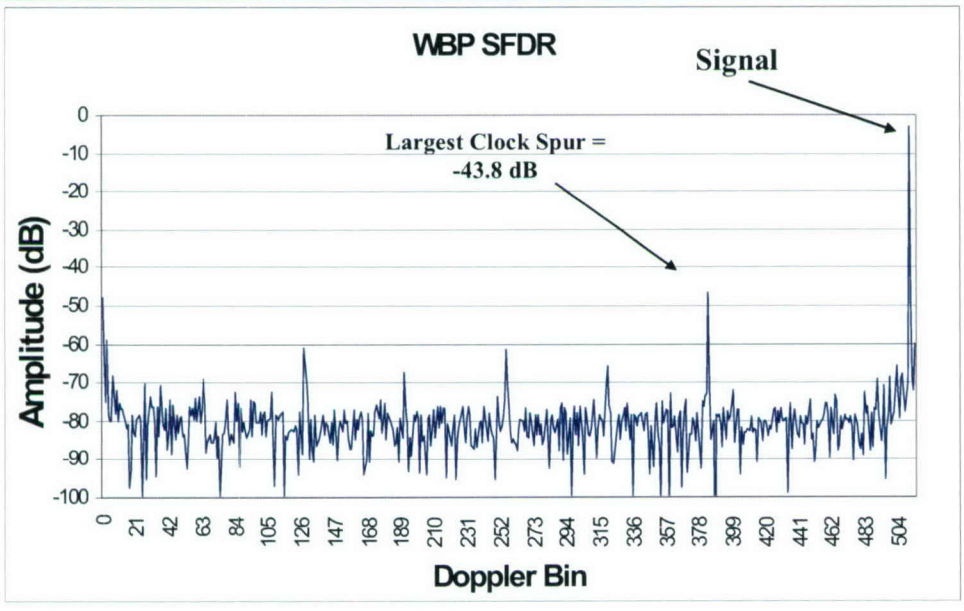

Figure 12: HBDP Measured Performance Wideband Channels

4. HBTX Introduction & Background

Raytheon has been supporting the Navy's Advanced Multifunction RF Concept (AMRFC) advanced technology program sponsored by ONR. The motivation for AMRFC is to reduce the surface combatant topside crowding and resulting RCS by minimizing the number of apertures required to support radar, communications, and Electronic Warfare (EW) mission needs.

As part of a technology development task under this program, Raytheon has developed a novel wide-band, dual-polarized, coincident phase-center element with excellent Cross-Polarization (X-pol) isolation to be available for populating the AMRFC high band transmit array. The Raytheon Electrically Short Crossed Notch (ESCN) element consists of an orthogonal pair of tapered crossed-notch antennas with a balanced feed to increase polarization purity. This wideband (notch) radiator provides excellent polarization performance vs. scan (better than other current notch capabilities). The current radiator operates from 7 to 21.2 GHz and will provide, without correction, X-pol isolation approaching 12 dB over a 60 degree conical scan volume.

Contemporary broadband phased array radiators generally show significant polarization degradation at large scan angles in the diagonal scan planes. This limitation can force the polarization compensation network to heavily weight a single polarization. The result for a transmit array is poor antenna radiation efficiency because the unweighted polarization must supply most of the antenna EIRP. This imbalance is largely removed with the polarization purity found in Raytheon's ESCN balanced-fed broadband radiator design.

4.1 HBTX Requirements and Goals

The primary goal of the High Band Transmit (HBTX) task was to design a dual-polarized, coincident phase center radiator with a 3:1 bandwidth that would maximize the element-level X-pol isolation. The original approach, requirements, and goals are shown in the Table below.

Table 4: Original HBTX Radiator Approach & Requirements

Approach	Requirements & Goals

• Design, fab, and test 2 MCAs
  • Single element fixture 3-9 GHz
  • One 2X MCA for 3 - 9 GHz
  • One 1X MCA for 6 - 18 GHz
• MCA's will be 31 x 31 element arrays
  • Center 11 x 11 elements connectorized
  • 2X array has 4 ports/element
  • 1X array will have 2 ports/element
  • Remaining elements terminated
	• 3:1 operating bandwidth
	• 60° conical scan volume
	• Dual polarized radiator
	• Coincident phase center for orthogonal pols
	• < 2.2 dB axial ratio (18.8 dB X-pol isol)
	• < 1.0 dB mismatch loss (2.66:1 VSWR)
	• Operate in Naval shipboard environment

The 2X (half-frequency) array was designed to operate over 3-9 GHz. Originally the 1X (full-frequency) array was to be designed to operate over 6-18 GHz; however, in late 2002, the Navy's Multiple Beam Aperture (MBA) Program was redirected to include a wideband array and the AMRFC radiator was chosen to be their baseline. Following our 15 Nov 02 Technical Interchange Meeting (TIM), ONR approved the direction of the AMRFC 1X array design to match the MBA 2x16 architecture, the MBA operating band of 7-21 GHz, and to adhere to the MBA lattice requirements.

The first 2X array populated all the elements with long fins. The individual fin length was 4.72-in. The diagonal plane results for this Mutual Coupling Array (MCA) indicated deep nulls in the

co-polarized (co-pol) response and significant levels of cross–polarization (X-pol) over the angles of interest. Initial far field and near field measurements of single-element long-fin radiator were shown and discussed in the 31 May 01 TIM. The mutual coupling data from the MCA was also shown and discussed. In the 31 Jul 01 TIM, we discussed the possibility of using an alternate notch geometry and showed some preliminary predictions; however, this avenue was not pursued. It was decided to focus upon our coincident phase center approach. Over the next few months, we investigated many fin configurations to try and reduce the diagonal plane X-pol and eliminate the diagonal plane co-pol nulls. Studies were conducted and a case was made for reducing the fin length to improve both the co-pol and X-pol response in the diagonal plane. This radiator is referred to as the Electrically Short Crossed-Notch (ESCN). It is shorter than traditional traveling wave notch antennas. The 2X ECSN fin length is approximately 1.2-in; hence, as a function of wavelength, the fin length is 0.3 λ at 3 GHz and 0.9 λ at 9 GHz. The initial test results showing the success of the ESCN single-element measurements and predictions were reported during the 23 Oct 01 TIM. The single-element measurements were extremely promising compared to the previous long-fin measurements. The shorter fin moved the diagonal plane co-pol null out beyond 70 degrees, and also greatly reduced the diagonal plane X-pol component. The next step was to produce the full 2X MCA with the 2X ESCN and take the embedded element patterns and swept gain measurements. In parallel with the radiator effort, a wideband balun to cover the 3:1 bandwidth and terminate even-mode fields, which corrupt the desired radiation, was also being designed. The 10 May 02 TIM detailed the vastly improved 2X ESCN MCA measurements and the preliminary balun design with the even-mode termination. The 2X ESCN and the initial even-mode attenuating balun measurements are summarized in the next section.

4.2 2X ESCN MCA Measured Embedded Element Performance

Raytheon fabricated a half-frequency, or twice-scale (2X), radiating element designed to operate over the 3-9 GHz band (vs. 7-21.2 GHz for the full scale or 1X). The iteration of the 2X MCA with ESCN elements only populated the center 11 x 11 connectorized region. The MCA's embedded element pattern and gain were measured in our near field and far field ranges. As shown in the Figure 13, the embedded element has excellent principal and diagonal plane co-pol and X-pol performance. The X-pol isolation in the principal planes exceeds 20 dB over scan angles of $\pm$ 70 degrees and the diagonal plane co-pol has principal plane-type performance over $\pm$ 70 degrees. The diagonal plane X-pol is significantly improved achieving X-pol isolation levels of 10 dB or better over a significant angular region, as wide as $\pm$ 50 degrees at some frequencies. Performance, both in principal and diagonal planes, is significantly better than results seen on other notch arrays in the published literature. The measurements of the AMRFC 2X short-fin MCA demonstrated the desired wideband performance with the desired polarization purity. The outstanding broadband performance and diagonal plane polarization purity is better than anything currently available.

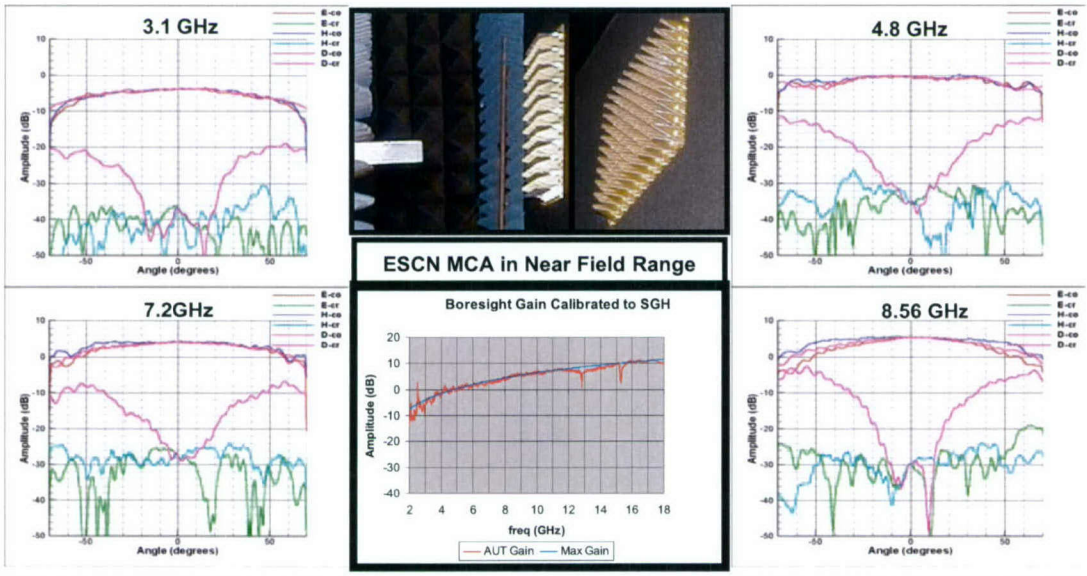

Figure 13: Raytheon's Electrically Short Crossed Notch (ESCN) MCA. Near-field measurements show excellent E, H, and diagonal (D)-plane co- and cross-polarization performance over a wide range of frequencies. The swept frequency (2-18 GHz) performance is also excellent.

The 2X ESCN MCA was also measured using a set of externally mounted baluns. There were 18 baluns that populated 9 dual-pol elements. This is shown in Figure 14 below.

The shape of the patterns measured with these baluns compared very well to those determined by analytically combining the ports; however, they exhibited 2-4 dB of loss due to the even-mode attenuation circuit. These results were reported at the 10 May 02 TIM and at the 2003 IEEE Phased Array Conference held in Boston, MA.

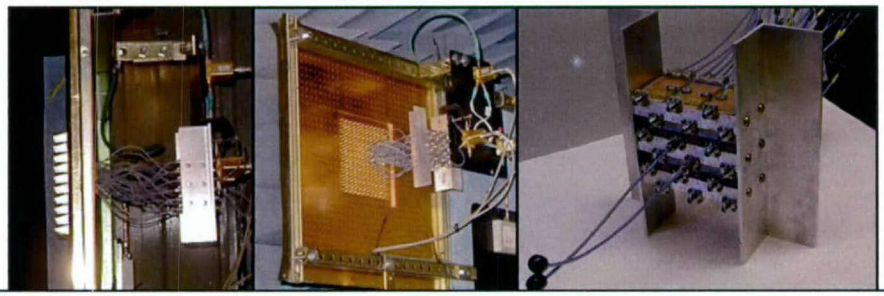

Figure 14: 2X MCA in the near field chamber with the external even-mode attenuating baluns using the initial balun design which exhibited 2-4 dB of loss.

4.3 Full Scale Array Design & Fabrication

The AMRFC radiator had been chosen to be adapted to meet the requirements for the Navy's Multiple-Beam Aperture (MBA) Program. This required a slight change in the 3:1 band for which we had originally been designing. Instead of 6-18 GHz, we were now designing for 7-21 GHz. This changed the lattice spacing; however, a more drastic change was the architecture. The MBA architecture was built around 2x16 radiator assemblies and required a radome.

We had already determined that a matching layer (basically an integrated sandwich radome) improved our match and also allowed us to make the fins even smaller, thereby further improving the X-pol isolation. This original integrated radome/matching layer was discussed at the 10 May 02 TIM. Many valuable lessons were learned from the building and testing the 2X array hardware. Among these was the relationship between fin length and X-pol isolation. In our 1X design this eventually transitioned to a single 45-mil teflon sheet or capacitive hat. The capacitive hat enables the fins to look electrically longer (improving the H-plane low frequency match) while actually being physically shorter (improving the X-pol isolation). The new ESCN fin for the 1X array design is now 0.277-in (277 mils) in length which, in terms of wavelength, ranges from approximately $\lambda/6$ at 7 GHz to $\lambda/2$ at 21 GHz.

The 1X array was fabricated in 2x16 blocks, with 3-D molded feed circuits that are fed by a pair of odd-mode baluns and are integrated into each cell. This architecture was chosen to match requirements for the MBA program. The 1X MCA will consist of eight 2x16 blocks. The basic 2x16 structure is shown in Figure 15.

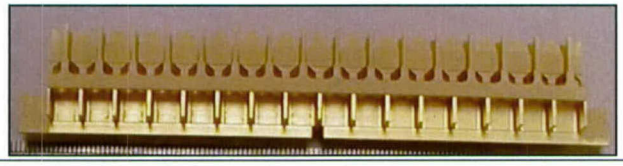

Figure 15: 1X 2x16 ESCN radiator block. End tabs are for mounting into the frame shown below.

The 16x16 MCA is shown in Figure 16. It consists of eight 2x16 radiator blocks mounted into the MCA frame. Each cell will have a feed and a pair of integrated balun circuits. The E-, H-, and diagonal plane embedded element patterns for this MCA were measured in our Near Field Chamber.

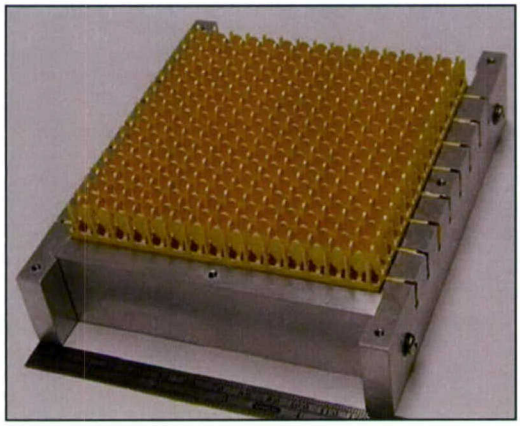

Figure 16: MCA built by mounting eight 2x16 ESCN radiator blocks into the MCA frame. It is populated with a feed and pair of baluns integrated into each cell. Embedded element measurements will be performed to determine the E, H, and diagonal (D)-plane co- and cross-polarization performance.

The predicted results for the 1X configuration indicate a VSWR < 1.6:1 and mismatch loss < 0.6 dB over the operating band for boresight and 30 degree scan angles. For the 60 degree scan angle case, the VSWR < 3:1 at the band edges (much better within the band) with a mismatch loss < 1.3 dB. The predicted axial ratio (AR) is excellent. The predictions for the principal and diagonal planes indicate AR < 5 dB (11 dB X-pol isolation) over most of the 60 degree scan

volume with AR < 2 dB (18 dB of X-pol isolation) in the principal planes at 21 GHz. Details are in the presentation charts included in Section 4.7.1

For each polarization, the crossed-notch radiator fins need to be fed in odd-mode. We also need a technique to attenuate the non-propagating even-mode to eliminate resonances. The new balun design meets both these requirements. The new balun design is a wideband 0/180 hybrid; thus, our new balun is a 4-port device. The balun is low loss and has a sum (even-mode) port we can terminate to eliminate the even-mode resonances. It is a simple design, easily implemented, with excellent predicted performance over the 3:1 bandwidth. The balun's input VSWR < 2:1 across the band with an insertion loss < 0.7 dB. The amplitude and phase balance for the balun's ports are excellent. The amplitude imbalance is < 0.4 dB across the band except at the band edges. In addition, the delta phase balance is ± 3 degrees across the band. The balun and feed are very important in the crossed-notch radiator design. As before, the details are in the presentation included in Section 4.7.2

This planned configuration and the associated predictions were reported at the 26 Aug 03 TIM. In addition, papers on the 2X ESCN MCA measurements, the balun design, and the prediction techniques were presented at the 2003 Raytheon RF Symposium as well as a paper at the 2003 IEEE Phased Array Conference. Once the hardware for the 1X ESCN MCA was fabricated, we prepared and presented papers at the 2004 Raytheon RF Symposium on the updated hardware, the improved balun, an N-Plexer design using the improved balun, and Polarization Compensation Techniques. All four 2004 Raytheon RF Symposium presentations are included in Section 4.7.1 – 4.7.4

Our AMRFC task was supported by a Joint Raytheon-University of Massachusetts Master's thesis project to quantify Polarization Compensation (pol-comp) algorithms and determine their performance using our measured phased array data. The pol-comp algorithms developed under this project were applied to the measured 2X MCA data with excellent results. The pol-comp algorithms were also used for analysis on the MBA program. This presentation is included in Section 4.7.4. Finally, a presentation detailing the preliminary status of the 1X MCA hardware was approved and presented at the 2004 IEEE Antennas & Propagation Conference.

4.4 HBTX Current Status and Conclusions

This radiator design is currently being used for the MBA demonstration array. As such, we continued to fabricate the 1X MCA and took embedded element patterns. These results were reported at the MBA Internal Critical Design Review (ICDR), held on 12 Aug 04.

The 1X MCA faced some complications. In an effort to produce a rudimentary scanning capability, many elements were connectorized. This produced problems that were a function of the interconnects vs. the radiator and balun. There were many locations of very high VSWR that could be directly traced to the various connector sites; however, these were in locations that would not exist in the actual MBA demo array. The MCA with the connectors is shown in Figure 17. The positions on the red lines are connectorized, the yellow positions are populated with feed and balun assemblies, and the yellow positions without a connector are terminated (load). All connector bar locations have the load resistor installed, but are not connected in the cells without the balun/feed circuitry. This creates several different types of cells. Some were completely open, some were terminated in the cavity, and some were terminated at the ends of

the coax. The connector bar and the coax cables were only required for 1X MCA and are not part of MBA Demo Array; however, they potentially caused significant measurement problems. The embedded element patterns had reasonable co-pol and X-pol performance (in regions where the swept gain cooperated). As expected, patterns were severely degraded in regions where there were resonances in the swept gain (and the corresponding high VSWRs). Much of the poor VSWR performance can be traced to locations in the connector bars and coax-cables that were used specifically in the MCA and are not part of demo array.

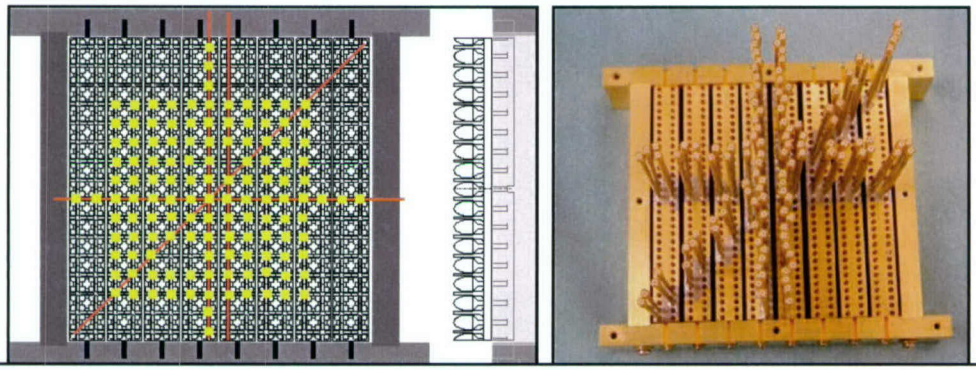

Figure17: Connectorization Configuration for the AMRFC 1X MCA

The basic radiator, balun, and feed designs are considered to be good; however, fabrication techniques should be revisited for future demo array builds. Figure 18 shows an example of the embedded element performance for a frequency where the coax and connector bar VSWR didn't corrupt the pattern. This shows good principal and diagonal plane co-pol and X-pol performance in spite of the VSWR problems. This performance should further improve once the VSWR issues are worked out.

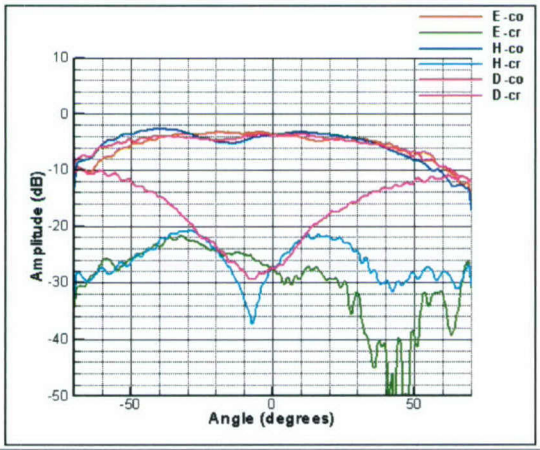

Figure 18: 1X MCA Embedded Element Pattern at 11.14 GHz. The E-, H-, and D-plane co-pol and x-pol performance are similar to what we previously measured with the 2X MCA. The actual gain level is indicative of the VSWR problems encountered in these measurements.

We gave 4 presentations at the 2004 Raytheon RF Symposium entitled:

- "7-21 GHz Wideband Phased Array Radiator - Embedded Element Performance"
- "Wideband Feed and Balun Assembly for ESCN Radiator"
- "7-21 GHz Wideband N-Plexer: Initial 2 & 3 Channel Designs"

- "Array Assessment for Polarization Compensation Due to Quantization Errors"

These presentations succinctly sum up the status at that time and also coincide with the HBTX completion. These presentations are referenced in Section 4.7 and can be provided upon request for added detail on the primary accomplishments of this task: the radiator design, the balun and feed design, and the polarization compensation studies. The following two sections also detail the various conference presentations, patent submissions, and TIM presentations supported under this task.

4.5 HBTX Conference Presentations and Patents

Results from this contract were presented at various Raytheon RF Symposiums, applicable IEEE Conferences, and were submitted for patents. The list below details these publications.

[1] "Wideband Phased Array Radiator – Embedded Element Performance", 2003 Raytheon RF Symposium, 21-24 Apr 2003, St. Petersburg, FL.
[2] "Even-Mode Attenuating Balun for Wideband Radiator", 2003 Raytheon RF Symposium, 21-24 Apr 2003, St. Petersburg, FL
[3] "Wideband Radiator Finite Element Modeling", 2003 Raytheon RF Symposium, 21-24 Apr 2003, St. Petersburg, FL.
[4] "7-21 GHz Wideband Phased Array Radiator - Embedded Element Performance", 2004 Raytheon RF Symposium, 2-5 May 2004, Boston, MA.
[5] "Wideband Feed and Balun Assembly for ESCN Radiator", 2004 Raytheon RF Symposium, 2-5 May 2004, Boston, MA
[6] "7-21 GHz Wideband N-Plexer: Initial 2 & 3 Channel Designs", 2004 Raytheon RF Symposium, 2-5 May 2004, Boston, MA.
[7] "Array Assessment for Polarization Compensation Due to Quantization Errors", 2004 Raytheon RF Symposium, 2-5 May 2004, Boston, MA.
[8] "Wideband Phased Array Radiator", 2003 IEEE Phased Array Systems & Technology Conference, 14-17 Oct 2003, Boston,, MA
[9] "7-21 GHz Wideband Phased Array Radiator", 2004 IEEE Antennas & Propagation Conference, 20-25 Jun 2004, Monterey, CA.
[10] Disclosure 00E112, 02E060, Wideband Electrically Short Crossed-Notch Radiator
[11] Disclosure 00E112A, Broadband Dual Polarized Slotline Feed
[12] Disclosure 03E068, Compact Wideband Feed Transition Assembly
[13] Disclosure 03E090, Wideband Marchand Microstrip Balun with Even Mode Termination
[14] Disclosure 03E091, N-Plexer Utilizing Raytheon's AMRFC Wideband Balun

4.6 HBTX Technical Interchange Meetings

The list below identifies the presentation material provided via the various Reviews, Displays, and Technical Interchange Meetings (TIMs) held over the duration of this contract. Data from these TIMs is referenced in the HBTX discussion.

1) Presentation, HiTeP Kick-off, 15 Aug 2000, at Raytheon (Sudbury)
2) Presentation, HBTX Technical Interchange Meeting, 28 Sep 2000, at Raytheon (Tewksbury)
3) Presentation, HBTX Technical Interchange Meeting, 08 Feb 2001, at NRL
4) Presentation, HBTX Technical Interchange Meeting, 31 May 2001, at Raytheon (Tewksbury)
5) Presentation, HBTX Technical Interchange Meeting, 31 Jul 2001, at NRL

6) Poster Presentation & Hardware Display, Dr. Coffey Review, 07 Sep 2001, at NRL
7) Presentation, HBTX Technical Interchange Meeting, 23 Oct 2001, at Raytheon (Sudbury)
8) Poster Presentation & Hardware Display, Annual Review, 08 Nov 2001, at NRL
9) Presentation, HBTX Technical Interchange Meeting, 10 May 2002, at NRL
10) Presentation, HBTX Technical Interchange Meeting, 15 Nov 2002, at NRL
11) Poster Presentation & Hardware Display, Annual Review, 13 Nov 2002, at NRL
12) Presentation, HBTX Technical Interchange Meeting, 26 Aug 2003, at NRL

All the TIM presentations were delivered to the Government in electronic format at the time of the meeting.

4.7 HBTX 2004 Raytheon RF Symposium presentations

For completeness and as a good summary of the status for the HBTX Task, reference to the four presentations given at the Raytheon 2004 RF Symposium is included in this section.

4.7.1 7-21 GHz Wideband Phased Array Radiator – Embedded Element Performance

Authors: K. Trott, R. Cavener, J. Biondi, R. Cummings, M. Deluca
Date: May 2004
Summary: The Electrically Short Crossed Notch (ESCN) element consists of an orthogonal pair of tapered crossed-notch radiators with a balanced feed to increase polarization purity. The ECSN provides excellent polarization performance vs. scan (better than current notch capabilities). The 2X (3-9 GHz) measured co-pol & x-pol embedded element patterns were discussed at the 2003 RF Symposium. This year's paper will discuss the 1X (7-21 GHz) design, predicted performance, fabrication, and measured embedded element patterns.

4.7.2 Wideband Feed and Balun Assembly for ESCN Radiator

Authors: R. Cummings , K. Trott, R. Cavener, J. Biondi, , M. Deluca
Date: May 2004
Summary: A new microstrip wideband balun (0°/180° balanced feed) and feed has been developed for use with the Electrically Short Crossed Notch (ESCN) radiator on the Advanced Multi-functional RF Concept (AMRF-C) program for the High Band Transmit Array (HBTX). This radiator/balun/feed assembly is being integrated into the Multi-Beam Apertures (MBA) array.

4.7.3 A 7-21 GHz Wideband N-Plexer: Initial 2 & 3 Channel Designs

Authors: M. Deluca , R. Cummings , K. Trott, R. Cavener, J. Biondi
Date: May 2004
Summary: Initial 2 and 3 channel N-Plexer designs have been created in HP ADS. These designs incorporate the AMRFC wideband four port balun data along with ADS filter models (5 stage 0.7 dB IL in pass bands). The 2 channel version breaks up the band into 7-12.5 GHz and 16-21GHz sections. Insertion Loss is lower than 2.2 dB across each channel and Isolation is greater than 10 dB at the band edges. The 3 channel version has an addition stage added, and breaks the band into 3 segments 8.5-10.5 GHz, 11.5-16Ghz, and 18-21GHz. The Insertion Loss for each channel is lower than 4.0 dB and the Isolation is greater than 10 dB.

4.7.4 Array Assessment for Polarization Compensation Due to Quantization

Authors: P. Driscoll, J. Bowen, B. Porter
Date: May 2004

Summary: Phased arrays can be used to increase the capabilities of modern communications systems. The required axial ratio at high scan angles for these applications is lower than what can be achieved with state of the art, circularly polarized radiating elements. If the amplitude and phase of the signals at the orthogonal linear ports can be controlled, then compensation can be applied to improve the axial ratio. This paper investigates the procedure and array hardware requirements for utilizing a polarization compensation scheme. Initial funding for this work was provided by the AMRFC program. The simulation tool developed has been utilized by MBA for initial predictions of G/T budget and hardware requirements. This work is applicable to other dual polarization architectures such as DD(X).